

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
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SUMAN DATTA)
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ROBERT S. CHAU)
Serial No.: unknown)
Filed: April 20, 2004)
For: A METHOD FOR MAKING A)
SEMICONDUCTOR DEVICE)
HAVING A HIGH-K GATE)
DIELECTRIC LAYER AND A)
METAL GATE ELECTRODE)
Art Unit: unknown
Examiner: unknown
Attorney Docket: P18609

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is being submitted under 37 C.F.R. §1.97(b). Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the references cited on that form. It is respectfully requested that the cited references be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement constitutes prior art or is otherwise material to patentability.

Respectfully submitted,

Dated: April 20, 2004



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Form PTO-1449 (Modified)		Atty Docket No.: P18609		Serial No.: Unknown		
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Justin K. Brask		
				Filing Date: April 20, 2004		
REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
	AA	6,063,698	Tseng et al.	438	585	
	AB	6,184,072 B1	Kaushik et al.	438	197	
	AC	6,420,279 B1	Ono et al.	438	785	
	AD	6,475,874 B2	Xiang et al.	438	396	
	AE	6,514,828 B2	Ahn et al.	438	240	
	AF	6,544,906 B2	Rotondaro et al.	438	785	
	AG	6,617,209 B1	Chau et al.	438	240	
	AH	6,617,210 B1	Chau et al.	438	240	
	AI	6,620,713 B2	Arghavani et al.	438	585	
	AJ	6,689,675 B1	Parker et al.	438	585	
	AK	6,696,327 B1	Brask et al.	438	197	
	AL	6,696,345 B2	Chau et al.	438	387	
	AM	US2002/0197790 A1	Kizilyalli et al.	438	240	
	AN	US2003/0032303 A1	Yu et al.	438	770	
	AO	US2003/0045080 A1	Visokay et al.	438	591	
FOREIGN PATENT DOCUMENTS						
		Document No.	Date	Country	Class	Sub-Class
	AP					Translation
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)						
	AQ	Polishchuk et al., "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion", www.eesc.berkeley.edu , 1 page				
	AR	Doug Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics", 2001 IEEE, 4 pages				
	AS	Lu et al., "Dual-Metal Gate Technology for Deep-Submicron CMOS Devices", dated April 29, 2003, 1 page				
	AT	Schwantes et al., "Performance Improvement of Metal Gate CMOS Technologies with Gigabit Feature Sizes", Technical University of Hanburg-Harburg, 5 pages				
	AU	Doczy et al., "Integrating N-type and P-type Metal Gate Transistors," Serial No. 10/327,293, Filed December 20, 2002				
	AV	Brask et al., "A Method for Making a Semiconductor Device Having a Metal Gate Electrode," Serial No. 10/704,497, Filed November 6, 2003				
	AW	Brask et al., "A Method for Etching a Thin Metal Layer", Serial No. 10/704,498, Filed November 6, 2003				
	AX	Brask et al., "A Method for Making a Semiconductor Device with a Metal Gate Electrode that is Formed on an Annealed High-K Gate Dielectric Layer", Serial No. 10/742,678, Filed 12/19/03				
	AY	Brask et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate Electrode", Serial No. 10/739,173, filed December 18, 2003				
	AZ	Brask et al., "A CMOS Device With Metal and Silicide Gate Electrodes and a Method for Making It", Serial No. 10/748,559, filed December 29, 2003				
	BA	Doczy et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate Electrode", Serial No. 10/748,545, filed December 29, 2003				
	BB	Shah et al., "A Method for Making a Semiconductor Device with a Metal Gate Electrode," Serial No. 10/805,880, filed March 22, 2004.				
	BC	Shah et al., "A Replacement Gte Process for Making a Semiconductor Device that Includes a Metal Gate Electrode," Serial No. 10/809,853, filed March 24, 2004.				
Examiner			Date Considered			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						

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